Response under 37 C.F.R. § 1.111
U.S. Application No.: 09/722,306

Attorney Docket No.: Q61090

REMARKS

Claims 1-11 are all the claims pending in the application.

As a preliminary matter, the Examiner has not indicated receipt or consideration of the references listed on form PTO/SB/08 A & B submitted with the Information Disclosure Statement filed on September 26, 2002. Therefore, Applicant respectfully requests the Examiner to acknowledge receipt of the Information Disclosure Statement filed on September 26, 2002 and initial and return a copy of the Form PTO/SB/08 A & B. For the Examiner's convenience, a copy of the Information Disclosure Statement as filed on September 26, 2002 is enclosed.

Applicant thanks the Examiner for indicating that claims 3 and 4 contain allowable subject matter. Applicant, however, does not acquiesce to any inferences or presumptions drawn from the Examiner's statement regarding the reasons for allowance. Moreover, Applicant respectfully holds the rewriting of claims 3 and 4 in abeyance until the arguments presented with respect to independent claim 1 have been reconsidered.

Claims 1, 2, and 5-11 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,126,956 to Komiya et al. (hereinafter "Komiya"). Applicant respectfully traverses in view of the comments below.

To be an "anticipation" rejection under 35 U.S.C. § 102, the reference must teach every element and recitation of the Applicant's claims. Rejections under 35 U.S.C. § 102 are proper only when the claimed subject matter is identically disclosed or described in the prior art. Thus, the reference must clearly and unequivocally disclose every element and recitation of the claimed invention.

Introduction

Of the rejected claims, only claims 1, 5, and 11 are independent. This response focuses at least initially on these independent claims. For example, claim 1, among a number of unique features recites:

> ...an available area for storing circuit elements of a circuit pattern being input;

> circuit pattern extracting means for making a comparison between a circuit element stored in said available area and a corresponding circuit element contained in one of the plurality of previously stored circuit patterns stored in said unavailable area, and extracting from the plurality of previously stored circuit patterns an extracted circuit pattern in which the comparison indicates an agreement between the compared circuit elements;
>
> copying means for copying the extracted circuit pattern into said available area in response to an input by an operator.

An illustrative, non-limiting embodiment of the present invention discloses an editing system capable of autonomously retrieving analogous ladder diagrams without bothering the operator with extra work and without wasting the storage capacity of an auxiliary storage device. For example, an unavailable storage area stores at least one circuit pattern that has been previously input and the available storage area stores a new circuit pattern (the pattern being input by the operator). A circuit pattern extracting means compares a circuit element in a circuit pattern stored in the available area with a corresponding circuit element in a circuit pattern stored in the unavailable area. If the circuit elements agree, the whole circuit pattern is extracted and displayed on the input screen and the operator is asked whether this circuit pattern should be utilized. If the operator decides to utilize this circuit pattern, then the whole extracted circuit pattern is copied into the available storage area. As a result, ladder diagrams are automatically retrieved without the operator having to manually search through a library of basic unit circuit patterns. This passage is provided by way of an example only and is not intended to limit the scope of the claims in any way.

In general, Komiya provides a method and an apparatus for displaying a ladder diagram for facilitating the debugging and maintenance of a sequence program. Moreover, Komiya teaches showing only the segments of the ladder diagram indicating the conditions for turning the relay on when the user enters the identification of a desired relay or a memory address

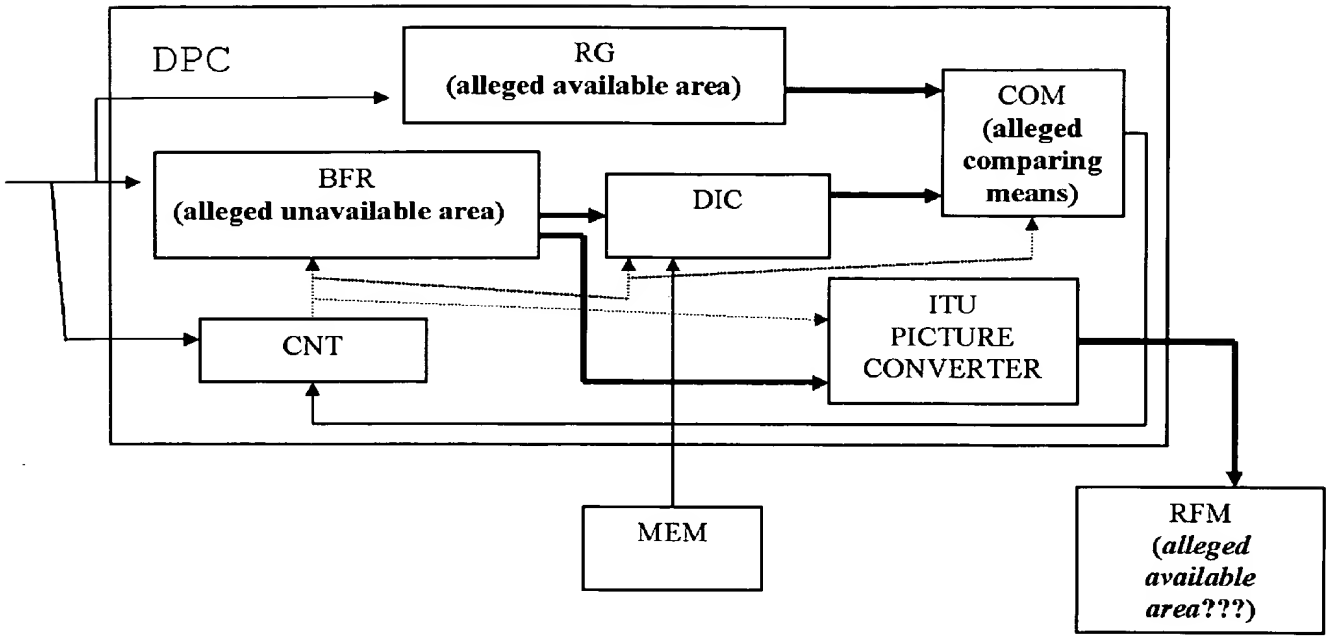
storing the state of the relay (col. 5, lines 46 to 58). Komiya teaches displaying ladder diagram segments indicating the conditions which turn a relay on by (1) entering either the identification of a relay such as a control relay or output relay or a memory address storing the state of the relay through use of an input device, (2) selecting the item of sequence data which indicates the conditions for turning the relay on, using the relay identification or memory address, and (3) displaying the ladder diagram segments that are based on the item of sequence data selected (col. 6, lines 45 to 58).

Examiner's Position

The Examiner now alleges that Komiya's display controller (DPC) meets the unique features of claim 1 recited above. In particular, the Examiner previously equated the DPC to the comparing means as recited in claim 1, and the character generator, the refresh memory, picture memory of Komiya to the available and unavailable areas, respectively, as recited in claim 1 (see *e.g.*, pages 5-6 of the Final Office Action dated March 9, 2004). In this Office Action, however, the Examiner alleges that the elements of the DPC meet the above recited unique features of claim 1.

Specifically, the Examiner now equates the buffer register (BFR) of the DPC to the unavailable area as recited in claim 1, the data register (RG) of the DPC to the available area as recited in claim 1, and the comparator (COM) of the DPC with the extracting means as set forth in claim 1 (see pages 2 to 3 of the Office Action). Finally, the Examiner alleges that "when comparison is finished and agreement between address and bit position for two items of data stored in register (RG) and buffer register (BFR) was reached, the data stored in BFR is converted into picture information, which is stored in the refresh memory (RFM)" (see page 4 of the Office Action).

In other words, the Examiner's position can be illustrated with the following diagram:



Applicant's Position

Applicant respectfully disagrees with the Examiner's position. Applicant respectfully incorporates herein by reference the arguments submitted in the Amendment under 37 C.F.R. §1.114 filed on September 8, 2004. Applicant further directs the Examiner's attention to the following additional points.

1. The RG and the RFM, cannot both be equated to the available area as set forth in claim 1.

First, Applicant respectfully submits that if, as alleged by the Examiner, the available area set forth in claim 1 is equivalent to the RG of the DPC, then Komiya clearly fails to teach or suggest "copying means for copying the extracted circuit pattern into said available area." The Examiner's position is technically inaccurate. As illustrated in the diagram above, it appears that for the purpose of storing circuit elements of a circuit pattern being input, the Examiner equates the available area to the register RG (last line on page 2 and first five lines on page 3 of the Office Action). For the purpose of copying the extracted circuit after the comparison, the

Examiner now alleges that the available area is equated to the RFM (last two lines on page 3 and first four lines on page 4 of the Office Action). The RFM and RG, however, are not equivalent elements and are clearly separate memory spaces, as illustrated in the diagram above and taught in Komiya. That is, Komiya does not teach or suggest storing pattern being input for comparison and copying the extracted circuit pattern into the same storage area.

These arguments were presented in the Submission under 37 C.F.R. § 1.114 (see page 12 of the Submission) and remain ***unrebutted*** by the Examiner. That is, the Examiner failed to explain how both the RFM and RG can be equivalent to the available memory.

Komiya teaches a Display Controller (DPC), which edits the data into picture information under the control of an editing program stored within a controller (col. 7, lines 59 to 61). Furthermore, Komiya teaches that within the DPC, the relay identification "CRA" is stored in a register RG (col. 8, lines 36 to 38). The relay identification or the memory address, at which the state of the desired relay is stored, is entered by the user on an input device such as the operator's panel or the manual data input device 301g (Fig. 8; col. 8, lines 23 to 30). Then, when the signal indicative of the relay identification enters the numerical control system, the data processor 301m delivers these signals to the universal display unit 301h (Fig. 8; col. 8, lines 31 to 36). The universal display unit 301h comprises a DPC, a refresh memory RFM, memory MEM, a character generator CG, a picture memory IMM, and a drive DVD, which receives the picture information output from IMM, for driving the cathode ray tube CRT (Fig. 8; col. 7, lines 21 to 38).

That is, Komiya teaches storing the relay identification "CRA" entered by the user into the RG of the DPC for comparison with relay identification output by the discriminator DIC and sends the results of such comparison to the controller CNT (col. 8, lines 53 to 56). If the two agree, the controller CNT causes a picture converter ITU to convert the unit of sequence program stored in the buffer register BFR into picture information, this picture information is then being stored in the RFM (Fig. 11; col. 8, lines 59 to 64). In short, in Komiya, if there is an agreement between the relay identification entered by the user and the unit of the sequence program code, this unit of the sequence program code is converted into picture information and this picture

information is stored in a RFM, and not in the register RG. The register RG is an element of the DPC, whereas RFM is a separate memory space and is not even an element of the DPC (see *e.g.* Figs 8 and 11 of Komiya). In short, in Komiya's system, a portion of the sequence program converted into picture form (allegedly the extracted circuit pattern) is stored in a RFM and not in the RG. The RG of the DPC stores only relay identification for further comparison with the sequence program code.

Furthermore, Applicant respectfully points out that the unit of sequence code stored in the BFR is converted into picture information and is not simply copied from one area into another area. That is, in Komiya, the CNT of the DPC causes a picture converter ITU to convert a unit of sequence code stored in BFR into picture information, and stores this picture information into the RFM (col. 8, lines 59 to 63). That is, in Komiya, a unit of sequence program code is stored in the BFR and the picture information is stored in the RFM. In short, the sequence code is not copied from BFR into RFM but is converted into picture information and it is the picture information that is stored in the RFM.

Therefore, "an available area for storing circuit elements of a circuit pattern being input...[and] copying means for copying the extracted circuit pattern into said available area..." as set forth in claim 1, is not disclosed by Komiya, which lacks storing input information and copying the extracted information into the same memory area. In Komiya, the user input is stored in RG of the DPC and the result of the comparison by COM of the DPC is converted and stored in a separate memory RFM. Moreover, in Komiya, the RFM stores picture information converted by ITU and the sequence code of the BFR is not simply copied into the RFM. For at least this exemplary reason, Applicant respectfully submits that claim 1 is patentably distinguishable from Komiya.

2. The converted information is not stored in the RFM in response to user input.

Next, Applicant respectfully submits that Komiya teaches that the sequence code in the BFR is converted by the ITU into the picture information, which is then stored in the RFM, based on the controller CNT and not in response to an input by an operator. For example, claim 1 recites: "copying means for copying the extracted circuit pattern into said available area in

response to an input by an operator." With respect to this exemplary feature of claims 1 and 5, the Examiner fails to address how the alleged storing picture information into the RFM is performed in response to user input (see page 4 of the Office Action). With respect to user input, the Examiner only alleges that "selecting each displayed pattern by an operator (col. 17-20)" (see page 5 of the Office Action) and "wherein if the nonagreement between the subject data from register (RG) and buffer (BFR) was found then a request for next input from operator is generated (col. 8, ll. 56-59)" (page 6 of the Office Action). In other words, it appears the Examiner equates Komiya's teaching of the operator inputting the identification of the desired relay or the memory address at which the state of the desired relay is stored, when the operator wishes to selectively display only the segments of the sequence program that constitute the ON conditions of the desired control relay or output relay, with the input by the operator as set forth in claim 1. Applicant respectfully disagrees.

Komiya teaches that when the operator wishes to selectively display only the segments of the sequence program that constitute the ON conditions of the desired control relay or output relay (col. 8, lines 13 to 21), the following procedure is implemented:

> *The user inputs the identification of the desired relay or the memory address, and the operator designates by a mode key, the ON conditions display mode for displaying a plurality of lines constituting the on conditions (col. 8, lines 22 to 30).*
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> *When the signals indicative of the relay identification and the inputted mode enter the numerical controller, they are delivered and stored in the RG of the DPC (col. 8, lines 31 to 38); in addition, the CNT of the DPC is set in the mode for selectively displaying only segments which constitute the ON conditions of the relay signal identification (col. 8, lines 38 to 41).*
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> *Also, one unit of the sequence program data extending from the operation code RD to the operation code WRT is transferred from ROM*

> *301d into the BFR of DPC (col. 7, lines 53 to 55 and col. 8, lines 41 to 44).*
>
> *When one input unit of the sequence program data enters BFR, the DIC of DPC discriminates the operation code WRT and goes to memory MEM (which stores the corresponding relationship between relay identifications and locations (data and bit positions of the data memory 301e storing the logical state 1 or 0 of the relays) from the table 301f) and reads out the relay identification corresponding to the programmed operand following the operation code WRT; this relay identification read out of MEM is delivered to the comparator COM of DPC (col. 7, lines 3 to 6, lines 51 to 53, and lines 67 to 68 and col. 8, lines 1 to 4 and lines 45 to 53).*
>
> *The COM of DPC compares the received relay identification from the DIC of DPC with the relay identification from the RG of DPC and sends the result of the comparison, namely whether the two identifications do or do not agree, to the CNT of DPC (col. 8, lines 52 to 56).*
>
> *6a) If the two identifications do not agree, then the CNT requests a transfer of the next input unit of the sequence program data and steps 3-5 are repeated (col. 8, lines 56 to 59).*
>
> *6b) If the two identifications do agree, the CNT causes the ITU of DPC to convert the unit of sequence program data stored in the BFR into picture information, and store this picture information into the RFM(col. 8, lines 59 to 63).*

In other words, in Komiya, the user enters only the relay identification, which is stored in the RG of DPC. Thereafter, the DPC goes through the entire sequence program, unit by unit, so

as to obtain all the segments that constitute the ON conditions of a desired control relay or output relay. This process is controlled by the CNT of the DPC. When the two identifications do not agree, the CNT requests the next unit of the sequence code from the ROM 301d to perform steps 3-5 described above (col. 7, lines 53 to 55 and col. 8, lines 56 to 59). That is, once the user enters the relay identification and the mode indicating the display of the ON conditions, Komiya teaches that the CNT of the DPC controls the whole process including converting the input unit of the sequence program stored in the BFR into picture information, and storing this picture information into the RFM. In short, what is alleged to be the user input is automatic transfer of the next unit of the sequence program data into the BFR.

Moreover, when there is an agreement between the identification relay obtained from MEM for the unit of the sequence program data of the BFR and the identification relay stored in RG, the CNT causes the ITU of the DPC to convert the unit of sequence program data into picture information and transfer that sequence information for storage into RFM. In other words, the unit of sequence program data from the BFR is not converted into the picture information and is not stored in the RFM in response to input by an operator but automatically in response to the signal of the CNT. That is, in Komiya, the operator does not control the conversion and transfer of the sequence code from BFR into RFM, when the COM outputs an agreement. For at least this additional exemplary reason, Applicant respectfully submits that claims 1, 5, and 11 are patentably distinguishable from Komiya.

In addition, claim 5 recites: "copying means for copying the extracted circuit pattern into said available area in response to another input by the operator." Komiya only teaches the initial input from the user (the identification of the desired relay and the mode key designating the ON conditions of the desired relay), which starts the process described above in steps 3 to 6. Komiya fails to teach any other user input, which can influence the process such as "copying the extracted circuit pattern into said available area in response to another input by the operator." For at least this additional exemplary reason, claim 5 is patentably distinguishable from Komiya.

Furthermore, claim 11 recites: "displaying said each extracted circuit pattern on a screen; selecting said each displayed circuit pattern by an operator; and copying the selected circuit

pattern into said second storage area". The Examiner alleges that selecting each displayed pattern by an operator is met by col. 17-20 of Komiya, (see page 5 of the Office Action). Since there is no col. 17-20 in Komiya, Applicant believes the Examiner meant col. 8, lines 17 to 20. Col. 8, lines 13 to 21 of Komiya recites:

> The foregoing description relates to a display operation for a case where the operator enters an ordinary request. Described next will be the processing which takes place in the display controller DPC shown in FIG. 11 when an operator wishes to selectively display only the segments constituting the ON conditions of a desired control relay or output relay. In the description, reference will be had to FIG. 11 showing a conceptual functional block diagram of the display controller DPC.

The passage of Komiya cited above only teaches that next, the processing in the DPC will be described when the operator wishes to selectively display only the segments constituting the ON conditions of a desired relay. In particular, Komiya only teaches the user entering the identification of the desired relay or memory address to obtain the display of only the segments constituting the ON conditions of a desired relay (col. 8, lines 22 to 29).

Komiya only teaches displaying the ladder diagram segments indicating the conditions which turn a relay on are displayed by 1) entering either identification relay or memory address, 2) selecting the item of sequence data which indicates the conditions for turning the relay on, using relay identification or memory address, and 3) displaying the ladder diagram segments that are based on the item of sequence data selected (col. 6, lines 46 to 57). In other words, by entering the relay identification or selecting an item of the sequence data, a ladder diagram segments are generated and displayed sequentially on the display in accordance with the order in which the sequence program was written (col. 8, lines 9 to 12) or a ladder diagram which includes the contacts for turning on the specified relay "CRA" is displayed and, at the same time, so is a ladder diagram corresponding to all segments which include the relays for driving these contacts. Input signals, namely HSM and JM, which are directly incorporated in the ladder, are

not displayed since these do not correspond to relays (Fig. 13, col. 9, lines 44 to 55). Komiya, however, does not disclose selecting said each displayed circuit pattern by an operator, and copying into the RFM based on whether the circuit pattern was selected.

The Examiner alleged that the process of comparing the stored new circuit pattern with each of said pre-stored plurality of circuit patterns and extracting each circuit pattern from said pre-stored plurality of circuit patterns that matches the stored new circuit pattern as set forth in claim 11 is taught by Komiya's comparison process in the DPC (see page 5 of the Office Action). If the foregoing were true, then clearly there is in Komiya no selecting of the resulting displayed ladder segments (col. 9, lines 2 to 5). That is, in Komiya, there is no teaching of selecting, by an operator, the extracted circuit patterns that are now displayed on the screen, and then copying these selected patterns into the second storage area as set forth in claim 11. For at least these additional exemplary reasons, claim 11 is patentably distinguishable over Komiya.

3. Summary.

In sum, Komiya teaches a program for displaying a ladder diagram of a sequence program or displaying particular parts of the sequence program depending on the request entered by the operator. Komiya, however, is not related to a ladder circuit editing system, where the system may retrieve analogous ladder diagrams.

Komiya teaches an editing program for displaying a sequence program or portions of the sequence program in a ladder diagram. Komiya, however, fails to teach or suggest storing a circuit pattern being input into the available area, and then copying the circuit pattern that matched into the available area in response to an input by an operator. Variations of these features are recited in the independent claims 1, 5, and 11. For example, claim 1 recites: "an available area for storing circuit elements of a circuit pattern being input; circuit pattern extracting means for making a comparison between a circuit element stored in said available area and a corresponding circuit element contained in one of the plurality of previously stored circuit patterns stored in said unavailable area, and extracting from the plurality of previously stored circuit patterns an extracted circuit pattern in which the comparison indicates an agreement between the compared circuit elements...and copying means for copying the extracted circuit

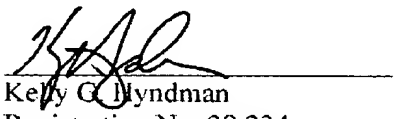
pattern into said available area in response to an input by an operator." For at least these exemplary reasons, Applicant respectfully submits that claims 1, 5, and 11 are patentably distinguishable from Komiya. Claims 2 and 6-10 are patentable at least by virtue of their dependency on claims 1 and 5, respectively. Therefore, Applicant respectfully requests this rejection of claims 1, 2, and 5-11 be withdrawn.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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